Drawings:

The attached sheet of drawing, which includes FIG. 1, replaces the original sheet including FIG. 1.

Attachment: Replacement Sheet

REMARKS/ARGUMENTS

Claims 1-45 are pending in this application. Claims 1, 13, 25 and 37 are independent claims.

Drawings

The drawings filed on 08/04/2003 were objected to by the Patent Office because of a typographical error in FIG. 1. The Replacement drawing has been attached to this Response to replace the original FIG. 1.

Claim Objections

Claims 1, 13, 25 and 37 were objected to because the Patent Office has alleged that the recitations of "predefining a slice"; "a first fabrication process"; "a second fabrication process"; "result" are not clear to what applicants intend to mean (Office Action, page 2). Applicant respectfully disagrees.

First, the Patent Office has failed to cite the legal authority under which the above objections were made. Applicant herein respectfully asks the Patent Office to pinpoint the section of *35 U.S.C.* under which the above claim objections were made.

Moreover, the above cited claim elements have been elaborated, for example, in FIG. 3 and paragraphs [0019] through [0034] of Specification and are understood by those of ordinary skill in the art.

Further, even though the Patent Office alleged that the above cited claim elements "are not clear to what applicants intend to mean," the Patent Office had no difficulty in giving detailed reasons when rejecting these claims under *35 USC § 102* (see below). This indicates that the Patent Office understood these claim elements, which contradicts the Patent Office's assertion that they "are not clear to what applicants intend to mean."

At least based on these reasons, the claims objections should be withdrawn.

Claim Rejections – 35 USC § 102

Claims 1-3, 5-15, 17-27 and 29-45 were rejected under 35 U.S.C. § 102(b) as being anticipated by Lee et al. ("Lee", U.S. Patent Number 5,500,805). Applicant respectfully traverses this rejection.

Anticipation requires the disclosure in a single prior art reference of each

element of the claim under consideration. *W.L. Gore & Assocs. v. Garlock*, 721 F.2d 1540, 220 USPQ 303 (Fed. Cir. 1983), cert. denied, 469 U.S. 851 (1984). Further, "anticipation requires the presence in a single prior art reference disclosure of each and every element of the claimed invention, arranged as in the claim." *Lindemann Maschinenfabrik GmbH v. American Hoist & Derrick Co.*, 730 F.2d 1452, 221 USPQ 481, 485 (Fed. Cir. 1984) (citing *Connell v. Sears, Roebuck & Co.*, 722 F.2d 1542, 220 USPQ 193 (Fed. Cir. 1983)) (emphasis added).

Independent Claim 1 recites an element of "a slice" (emphasis added). As indicated in Specification,

> A slice is a pre-manufactured chip in which all silicon layers have been built, leaving the top metal layers to be completed with the customer's unique IP. For example, RapidSlice™ developed by LSI Logic Corp. is an instance of a slice. One or more slices may be built on a single wafer. It is understood that a slice may include one or more bottom metal layers or may include no metal layers at all. In a preferred embodiment of the prefabrication step, the diffusion processes and the early-metal steps are carried out in a wafer fab. That is, the base characteristics, in terms of the IP, the processors, the memory, the interconnect, the programmable logic and the customizable transistor array, are all laid down and prediffused, and the early-metal components of the stack are manufactured. However, a slice is still fully decoupled because the customer has not yet introduced the function into the slice (page 6, paragraph [0016]),

and

> A slice is a constrained specification. A slice is an abstract specification of all IP, characteristics of interconnect, memory structures, I/O's, a transistor array, embedded programmable logic (if there is any), and the like. All these elements are pre-specified before any functional exploitation of the resources on the slice is commenced. The fact that a slice is a constrained environment suggests that the problem of readily mapping a pre-specified slice definition onto different fabrication processes may be computationally tractable. That is, it may be possible to take the slice definition, irrespective of what the slice ultimately will be used for in a final product, and apply the slice definition to any of several alternative fabrication

> processes, possibly from alternative foundries (the sources of supply for the slice) (page 7, paragraph [0019]).

In rejecting Claim 1, the Patent Office has relied on col. 12, ll. 62-63 and col. 13, ll. 7-24 of Lee for teaching this element (Office Action, page 3, ll. 8-9 from bottom). Applicant respectfully disagrees.

Col. 12, ll. 62-63 of Lee recites "each other and meet the requirements of the designer as specified during specification step 501," and col. 13, ll. 7-24 of Lee recites:

> FIG. 2 shows that, in accordance with this invention, the process parameters (such as may be defined by Spice parameters and design rules) for each alternate source fabrication facilities, equalize the performance of devices to be fabricated by each alternate source, and generate a single library with he same functionality and timing performance in order to generate models for steps 502 through 505 of FIG. 2. In this manner a customer with a desired function uses library 509 which is applicable to the plurality of alternate source fabrication facilities. Further, by using the same place and route step 505, correspondingly similar wire lengths are assured among the corresponding ASICs fabricated by alternate sources. During the mask making process, masks are adjusted (in mask adjust steps 506-1 through 506-N) to the minimum design rules for each alternate source, allowing each alternate source to produce the smallest (and thus least costly) integrated circuit permitted under its design rules.

Nowhere in Lee was "a slice," as recited in Claim 1, taught, disclosed or suggested.

Furthermore, Claim 1 recites "platform-based design." In contrast, Lee pertains to "gate arrays, embedded arrays, and standard cells" (col. 1, ll. 16-17). When rejecting Claim 1, the Patent Office has analogized "platform-based design" to array based design (Office Action, page 3, ll. 11 from bottom). Applicant respectfully disagrees. The Patent Office herein is respectfully directed to FIG. 1 and paragraphs [0010] through [0015] of Specification to see the difference between the platform and the gate array. Platform-based design *cannot* be analogized to array-based design.

At least based on the foregoing-described reasons, the rejection of Claim 1 should be withdrawn, and Claim 1 should be allowed.

Independent Claims 13 and 25 were essentially rejected based on the same

rational as applied to Claim 1. Since Claim 1 is allowable, Claims 13 and 25 are allowable.

Claims 2-3 and 5-12 depend from Claim 1 and are therefore allowable due to their dependence upon Claim 1. Claims 14-15 and 17-24 depend from Claim 13 and are therefore allowable due to their dependence upon Claim 13. Claims 26-27 and 29-36 depend from Claim 25 and are therefore allowable due to their dependence upon Claim 25.

Independent Claim 37 recites:

> 37. A computer-readable medium having stored thereon a database having a data structure, said data structure comprising:
> (a) a first field containing data representing a slice definition;
> (b) a second filed containing data representing a first set of design rules with which said slice definition is mapped to a first fabrication process;
> (c) a third field containing data representing a second set of design rules with which said slice definition is mapped to a second fabrication process; and
> (d) a fourth field containing data representing a result of computed comparison between results of said two mapping.

When rejecting Claim 37, the Patent Office has apparently mistakenly treated it as Claim 25 (Office Action, page 5, ll. 8-20). Therefore, the rejection of Claim 37 should be withdrawn, and Claim 37 should be allowed.

Claims 38-45 depend from Claim 37 and are therefore allowable due to their dependence upon Claim 37.

Claim Rejections – 35 USC § 103(a)

Claims 4, 16 and 28 were rejected under 35 U.S.C. § 103(a) as being unpatentable over Lee in view of Chen et al. ("Chen", U.S. Patent Number 6,757,882). Applicant respectfully traverses this rejection.

"To establish a *prima facie* case of obviousness, three basic criteria must be met. First, there must be some suggestion or motivation, either in the references themselves or in the knowledge generally available to one of ordinary skill in the art, to modify the reference or to combine reference teachings. Second, there must be a reasonable expectation of success. Finally, the prior art reference (or references when

combined) must teach or suggest all the claim limitations." (emphasis added) (MPEP § 2143). If an independent claim is nonobvious under 35 U.S.C. 103, then any claim depending therefrom is nonobvious. (emphasis added) *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988).

As indicated in the foregoing *Claim Rejections – 35 USC § 102* section, Lee fails to teach, disclose, or suggest the element of "a slice," as claimed in Claims 1, 13 and 25. Furthermore, Chen also fails to teach, disclose, or suggest the above-indicated claim element. Thus, independent Claims 1, 13 and 25 are nonobvious under 35 U.S.C. § 103.

Claims 4, 16 and 28 depend from Claims 1, 13 and 25, respectively, and are therefore nonobvious due to their dependence. Thus, the rejection should be withdrawn, and Claims 4, 16 and 28 should be allowed.

CONCLUSION

In light of the foregoing, Applicant respectfully requests that a timely Notice of Allowance be issued in the case.

Respectfully submitted on behalf of
LSI Logic Corporation,

Dated: May 25, 2005

By: _____
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Attachment